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APPROVALS		TYPE PROCUREMENT
J.C. Wolter W.S. Wright	# SPECIFICATION	DATE 15 October 1964
		SUPERSEDES SPEC. DATED:
		REV. LTR. / PAGE 1 of 7

TITLE

COMPUTER BUFFER UNIT, GUIDANCE AND NAVIGATION

E.O. 310116

1. SCOPE

1.1 Scope.- This specification covers the requirements for a Guidance and Navigation Computer Buffer Unit, hereinafter referred to as the G&N buffer. The G&N buffer shall form a part of the Digital Test Command System (DTCS) which is the up-link portion of the Automatic Checkout Equipment (ACE). The ACE will be used as ground support equipment for the Apollo spacecraft. The G&N buffer shall receive remotely generated digital test commands from the control room via the DTCS and shall store, verify, and shift out G&N data in appropriate format to the G&N on-board computer. Figure 1 shows a functional diagram of the G&N buffer.

2. APPLICABLE DOCUMENTS

2.1 Applicability.- The applicable documents for the G&N buffer shall be as follows:

MC 901-0675 15 October 1964	Digital Test Command System

3. REQUIREMENTS

3.1 Materials, Parts and Processes.- The materials, parts and processes for the G&N buffer shall be as specified in Specification MC 901-0675.

3.2 Design and Construction.- The G&N buffer shall be designed to meet the requirements of Specification MC 901-0675 and the following.

3.2.1 Dimensions.- The dimensions of the G&N buffer shall be as shown on the specification control drawing (SCD).

3.2.2 Electrical Design.- The electrical requirements of the G&N buffer shall be in accordance with Specification MC 901-0675 and herein.

3.2.2.1 G&N Buffer/Receiver-Decoder Interface.- The G&N buffer shall interface with the receiver-decoder as shown in Figure 1 and in accordance with the receiver-decoder/G&N buffer interface requirements of Specification MC 901-0675.

3.2.2.2 G&N Buffer/Apollo Guidance Computer (AGC) Interface.- The G&N buffer/AGC interface shall be in accordance with the G&N buffer/AGC interface requirements of Specification MC 901-0675.

3.2.2.3 Test Points.- The G&N buffer shall include test points for bench maintenance level malfunction isolation and component performance tests. All test points shall be included in the connectors provided for interfacing with the enclosure in which the G&N buffer is located. Test point selection shall be negotiated with NAA/S&ID.

3.3 Performance Requirements.-

3.3.1 General.- Three checks shall be made on the system in sequential order as follows and reported to the CSR in the same sequence. A go condition by one check shall enable the next check to be made. The flow, control, and check of information to, from, and within the G&N buffer shall be as shown in Figure 1.

(a) A buffer not busy check shall be made to indicate that the G&N buffer is not in the process of shifting out information whenever the G&N buffer is addressed.

(b) A mode-check shall be made to determine whether one and only one mode has been selected.

(c) A buffer check shall compare the contents of the G&N buffer with those of the DTCS staticizing register comparison gates. A check shall also be performed in the comparison gates to determine whether the buffer register stages are malfunctioning. The buffer shall be sampled only during a portion of the time in which the G&N module is addressed. At the end of the buffer sample time, all further action is enabled. Figure 1 is a functional diagram of the G&N buffer.

3.3.2 Mode Decoder.- The module shall operate in two modes which shall be decoded in the G&N buffer. DTCS register bit positions 2^2 and 2^1 shall control the selection of the mode. If $2^2 = 1$ and $2^1 = 0$ the action shall be to check, then load, the buffer memory (LBM). If $2^2 = 0$ and $2^1 = 1$ the action shall be to check the buffer memory and execute (EXC) by shifting out information to the Apollo Guidance Computer (AGC) if coincidence is achieved. Figure 2 shows the command message format.

3.3.3 Transfer Gates.- On receipt of an indication that only one mode has been selected, and a selection of theload buffer memory mode of operation, the transfer gates shall be enabled and 16 data bits shall be transferred in parallel to the G&N buffer regardless of the results of the coincidence check.

3.3.4 Comparison Gates.- The contents of the G&N buffer shall be compared with those of the DTCS staticizing register in the comparison gates. If there is coincidence, a buffer O.K. signal shall be sent to the CSR if either mode is selected. In the execute mode, coincidence shall start the clock and lack of coincidence shall reset the buffer register. The clock shall not be started until the termination of the end-of-word (8.0 plus or minus 2.0 microseconds) pulse. A check shall also be performed in the comparison gates to determine whether the buffer register stages are malfunctioning.

3.3.5 Counter and Clock.- The counter and clock circuitry shall contain a binary 16-counter to count the number of bits that are shifted out of the buffer. When a count is initiated, and until it is terminated, a flip-flop shall be set. When this flip-flop is in the reset position, a buffer not busy shall be sent to the CSR if the G&N select and group check pulses are both received. The lack of this signal shall inhibit the transfer gates from passing data.

3.3.6 G&N Buffer Register.- The G&N buffer shall be a sixteen stage shift register to accept data in parallel form and shift it out in serial form. The stages shall be reset if a comparison is made with the DTCS register and coincidence is not achieved when operating in the execute mode.

3.3.7 Power.- The G&N buffer shall contain power supplies necessary for its own circuits. The input power line and return line shall be electrically isolated from the G&N buffer signal ground and chassis ground.

3.3.8 System Normalizer.- The G&N buffer shall contain a normalizer circuit to insure re-setting of the control flip-flops when power is turned on.

3.4 Environmental Requirements.- The environmental requirements for the G&N buffer shall be as specified in Specification MC 901-0675.

3.5 Service and Storage Life.- Service and storage life of the G&N buffer shall be as specified in Specification MC 901-0675.

3.6 Reliability Requirements.- The reliability requirements for the G&N buffer shall be as specified in Specification MC 901-0675.

3.6.1 Numerical Reliability Objective.- The G&N buffer shall be of such design and construction that the mean-time-between-failure (MTBF) shall not be less than 220,000 hours. A failure to comply with this objective shall be negotiated with NAA/S&ID before taking corrective action.

3.7 Identification.- The identification of the G&N buffer shall be as specified in Specification MC 901-0675.

4. QUALITY ASSURANCE PROVISIONS.- Quality assurance provisions for the G&N buffer shall be as specified in Specification MC 901-0675.

5. PREPARATION FOR DELIVERY.- The preparation for delivery of the G&N buffer shall be as specified in Specification MC 901-0675.

6. NOTES.- Notes for the G&N buffer shall be as specified in Specification MC 901-0675.

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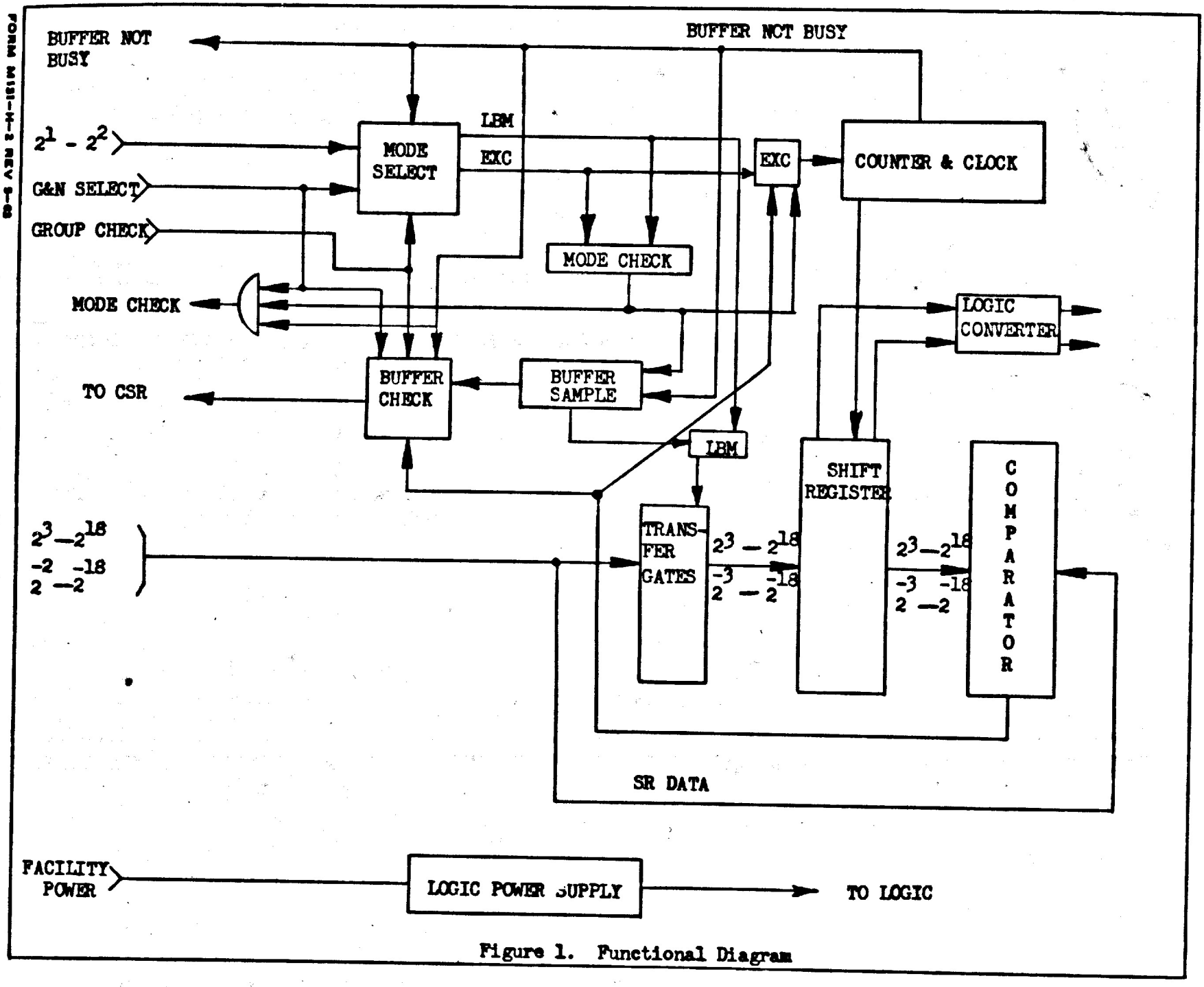

Figure 1. Functional Diagram

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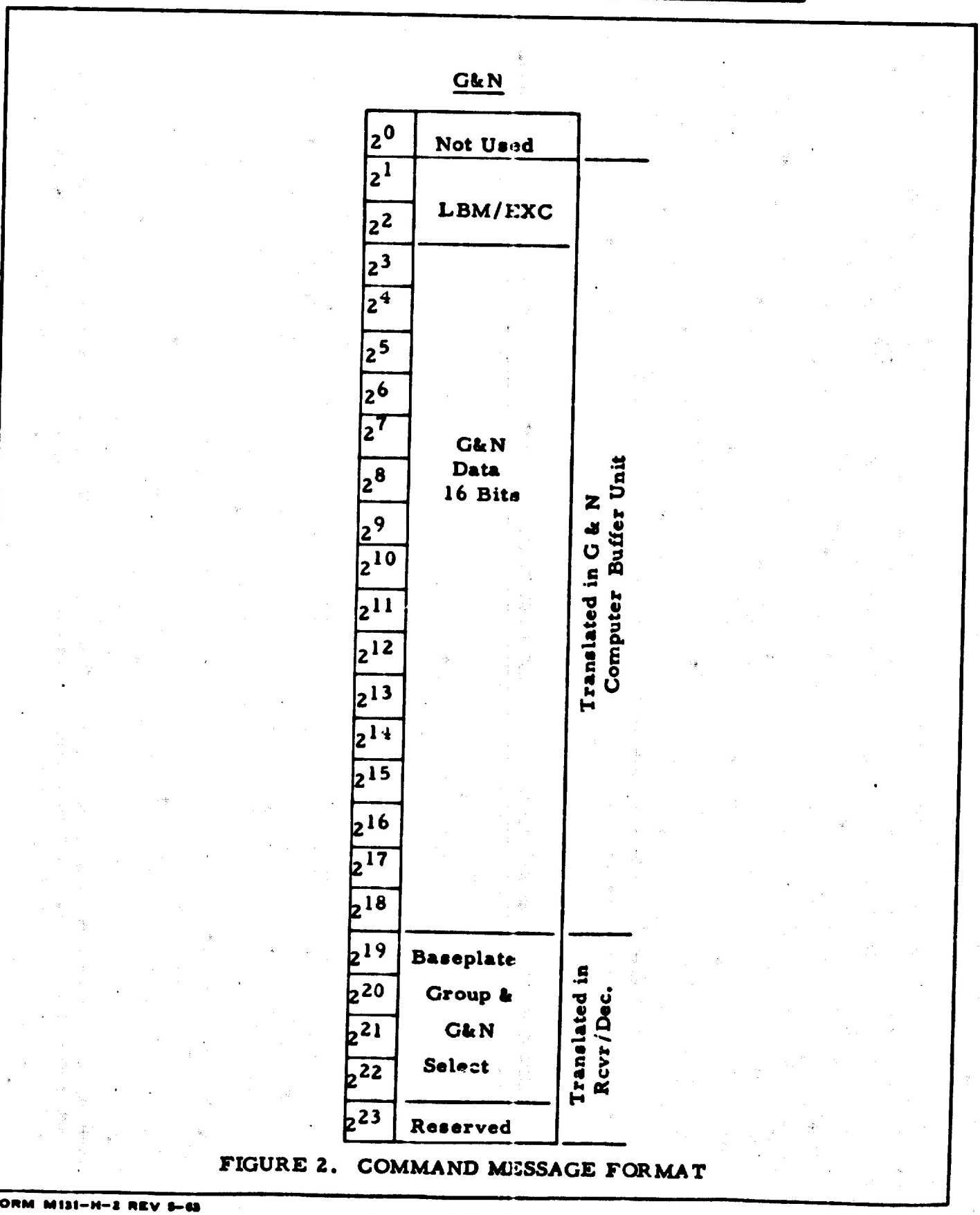

FIGURE 2. COMMAND MESSAGE FORMAT

STANDARDS
REVISION RECORD SHEET

REASON FOR REVISION

ENGINEERING REQUEST

DISPOSITION RECORD

INTERCHANGEABILITY AFFECTED YES [ ] NO [X]

REVISED FROM	REVISED TO
SHEET 1	SHEET 1
NAS622-TC2 NAA PROCUREMENT SPECIFICATION: MC 901-0666	Added ASL note NAS 622-CT-2 NAA PROCUREMENT SPECIFICATION: MC 901-0666A
SHEET 2	SHEET 2
J 202 J200 Back View .376 ± .001 Dia Hole .875 deep Counterbore .568 + .008 - .001 .062 deep	Added circuit breaker J200 J202 "Teflon Insert ... " as shown"
SHEET 3	SHEET 3
J203 Pin numbers 1 through 61 and function	Deleted

E.O. 328083

DIVISION S&ID	TITLE COMPUTER BUFFER UNIT, GUIDANCE AND NAVIGATION	REVISION DATE 2/3/65 "A"
CHG BY O. Davis		ME 901-0666 Sheet 1 of 1

FORM 122-X-2